Claims

1. An electronic circuit including a first semiconductor device and a second semiconductor device on a mounting substrate, wherein

the mounting substrate includes a plurality of mounting substrate lines which are connected in common with external terminals of a plurality of bits of the first semiconductor device and external terminals of a plurality of bits of the second semiconductor device for every bit,

the mounting substrate lines have lengths thereof from the external terminals of the first semiconductor device to the external terminals of the second semiconductor device made unequal for respective bits,

assembling lines which reach connecting electrodes of a semiconductor chip from the external terminals of the second semiconductor device have made lengths thereof unequal for respective bits, and

the unequal lengths of the mounting substrate lines have a relationship which offsets the unequal lengths of the assembling lines.

2. An electronic circuit according to claim 1, wherein the first semiconductor device is formed of a synchronous memory, the second semiconductor device is formed of a data processor which is capable of getting access to and controlling

the synchronous memory, and the data processor performs parallel inputting/outputting of access data of a plurality of bits between the data processor and the synchronous memory via the mounting substrate lines.

3. An electronic circuit according to claim 2, wherein the external terminal of a plurality of bits of the synchronous memory has data inputting/outputting timing thereof synchronized with the clock signal, and the data processor acquires data outputted from the synchronous memory in synchronism with the clock signal which is outputted from the synchronous memory.

4. An electronic circuit according to claim 3, wherein the second semiconductor device includes the package structure in which a large number of solder ball electrodes are annularly formed on the package substrate in a plurality of rows as external terminals, wherein unequal lengths of the assembling lines in the inside of the package substrate have the difference integer times as large as a pitch in the row direction of the solder ball electrode.

5. An electronic circuit according to claim 1, wherein the first semiconductor device has lengths of the assembling lines thereof from the external terminals thereof to connection electrodes of the semiconductor chip made equal to each other.

6. A semiconductor device which mounts a semiconductor

chip on a package substrate, wherein

the semiconductor chip includes a determination circuit which performs a determination operation using a reference potential supplied from a predetermined pad electrode,

the package substrate includes a first conductive layer which is used for the connection with the pad electrodes of the semiconductor chip, a second conductive layer which is used as a ground plane, a third conductive layer which is used as a power source plane, and a fourth conductive layer which is used for the connection with the mounting substrate, and

the third conductive layer includes a power source plane which is connected with the determination circuit and lines for the reference potential, wherein the lines for the reference potential are arranged in a state that the lines for the reference potential are surrounded by the power source plane.

7. A semiconductor device according to claim 6, wherein the second conductive layer is arranged between the first conductive layer and the third conductive layer.

8. An electronic circuit including a semiconductor device on a mounting substrate, wherein

the mounting substrate includes a first conductive layer on which a wiring pattern is formed, a second conductive layer which is used as a ground plane, a third conductive layer which is used as a power source plane, and a fourth conductive layer

on which a wiring pattern is formed, and

the ground plane and the power source plane include specified regions where via holes or through holes are not formed in a penetrating manner with a width equal to or larger than one pitch of external terminals which are arranged on the semiconductor device.

9. An electronic circuit according to claim 8, wherein external terminals of the semiconductor device are joined to the wiring pattern of the first conductive layer, a ground wiring pattern of the first conductive layer is joined to a ground plane of the second conductive layer through via holes or through holes, a power source wiring pattern of the first conductive layer is joined to the power source plane through via holes or through holes which penetrate the second conductive layer, and a predetermined signal wiring pattern of the first conductive layer is joined to a wiring pattern of the fourth conductive layer through via holes or through holes which penetrate the second conductive layer and the third conductive layer.

10. An electronic circuit according to claim 9, wherein the specified region of the ground plane has joining portions with the via holes or the through holes which are connected with the ground wiring pattern of the first conductive layer.

11. An electronic circuit according to claim 10, wherein the specified region of the power source plane has joining

portions with the via holes or the through holes which are connected with the power source wiring pattern of the first conductive layer.

12. An electronic circuit according to claim 11, wherein the specified regions are positioned in the vicinity of corner portions of the rectangular semiconductor device.

13. An electronic circuit according to claim 9, wherein the semiconductor device includes the package structure in which a large number of solder ball electrodes are annularly arranged in a plurality of rows on the package substrate,

the wiring pattern of the first conductive layer includes annularly arranged lands to which the solder ball electrodes are connectable in a plurality of rows, and

the via holes or the through holes which are connected to the ground plane or the via holes or the through holes which are connected to the power source plane are arranged outside an outer peripheral portion or the inside of the inner peripheral portion of the region where the lands are annularly formed.

14. A mounting substrate on which a semiconductor device is mounted, wherein

the mounting substrate includes a first conductive layer on which a wiring pattern having lands to which external terminals of the semiconductor device are connectable is formed, a second conductive layer which is exclusively used

on a ground plane, a third conductive layer which is exclusively used on a power source plane, and a fourth conductive layer on which a wiring pattern is formed, and

the ground plane and the power source plane have specified regions where the via holes or the through holes do not penetrate at a width of one pitch or more of the land.

15. A mounting substrate according to claim 14, wherein the ground wiring pattern of the first conductive layer is joined to the ground plane via via holes or through holes, a power source wiring pattern of the first conductive layer is joined to the power source plane via via holes or through holes which penetrate the second conductive layer, and the predetermined signal wiring pattern of the first conductive layer is joined to the wiring pattern of the fourth conductive layer via via holes or through holes which penetrate the second conductive layer and the third conductive layer.

16. A mounting substrate according to claim 15, wherein joining portions where the via holes or the through holes are joined to the ground wiring pattern of the first conductive layer are formed on specified regions of the ground plane.

17. A mounting substrate according to claim 15, wherein joining portions where the via holes or the through holes are joined to the power source wiring pattern of the first conductive layer are formed on specified regions of the power source plane.

18. An electronic circuit including a plurality of semiconductor memory devices and a semiconductor control device which is capable of getting access to and controlling the semiconductor memory devices on a mounting substrate, wherein

the mounting substrate includes a power source plane of a terminating power source for terminating lines which connect the semiconductor memory devices and the semiconductor control device by way of terminating resistances,

the semiconductor memory devices are mounted closer to the power source plane of the terminating power source than the semiconductor control device,

to the power source plane of the terminating power source, terminating resistances which are connected with the lines and a plurality of first stabilizing capacities which are arranged close to the terminating resistances are connected in a dispersed manner, and

a second stabilizing capacity which is larger than the first stabilizing capacities is connected to an end portion of the power source plane remote from the supply end which supplies the terminating power source.

19. An electronic circuit according to claim 18, wherein the power source plane of the terminating power source has a shape which includes rectangular corner portions in the rectangular mounting substrate, the supply end of the

terminating power source is arranged in the vicinity of the rectangular corner portion, and the power source plane of the terminating power source extends toward both sides of the supply end of the terminating power source.

20. An electronic circuit according to claim 18, wherein among the lines, the one-way line having a branch to which a plurality of semiconductor memory devices excluding a CLK, a /CLK is connected in common has a terminating resistance thereof connected to a route having a longer route length starting from the semiconductor control device.

21. An electronic circuit according to claim 18, wherein among the lines, the one-way lines having a branch to which a plurality of semiconductor memory devices excluding a CLK, a /CLK is connected in common, include lines which have terminating resistances thereof joined to the route having the longer route length starting from the semiconductor control device and lines which have terminating resistances thereof joined to the shorter route in mixture, and

a maximum value of the difference of the route length between the longer route in the one-way line which has the terminating resistance thereof joined to the shorter route and the shorter route is set to a minimum value or less of the difference of the route length between the shorter route in the one-way line which has the terminating resistance thereof joined to the longer route and the longer route.

22. An electronic circuit according to claim 21, wherein the one-way line having a branch is a line which transmits commands and addresses to the plurality of semiconductor memory devices from the semiconductor control device.

23. A semiconductor device which mounts a semiconductor chip on a package substrate, wherein

the semiconductor chip includes a phase locked loop circuit or a delay locked loop circuit,

the package substrate includes a first conductive layer which is used for connection with pad electrodes of the semiconductor chip, and

the first conductive layer includes a power source line which supplies a power source to the phase locked loop circuit or the delay locked loop circuit, and clock lines which supply clock signals to the phase locked loop circuit or the delay locked loop circuit, wherein the power source line and the clock line are spaced apart from each other with a distance larger than a minimum distance size of lines in the first conductive layer.

24. A semiconductor device according to claim 23, wherein the package substrate includes a second conductive layer which is used as the ground plane exclusively, and a third conductive layer which is used as the power source plane exclusively, wherein the power source line which supplies the power source to the phase locked loop circuit or the delay locked loop

circuit on the third conductive layer is arranged independently from other power source planes.

25. A semiconductor device which mounts a semiconductor chip on a package substrate, wherein

the semiconductor chip includes converters of either one or both of a digital analog converter and an analog digital converter,

the package substrate includes a first conductive layer which is used for connection with pad electrodes of the semiconductor chip, a second conductive layer which is used as the ground plane, a third conductive layer which is used as the power source plane, and a fourth conductive layer which is used for connection with the mounting substrate,

on the third conductive layer, power source planes for the converters are separated from the power source plane for other circuits, and

on the first conductive layer, signal lines for converters are formed at positions where the signal lines for converters are overlapped to the power source plane for the converters.

26. A semiconductor device according to claim 25, wherein

the converter includes a circuit which adds a constant current from a constant current source circuit to an output node via a switch,

the power source plane for converter which is formed on

the third conductive layer is assumed as the power source plane of the constant current source circuit, and

the power source plane of the circuit which controls the switch is formed on the fourth conductive layer separately from the power source plane of the constant current source circuit.

27. A semiconductor device according to claim 26, wherein the power source plane for converter which is formed on the third conductive layer and the power source plane of the circuit for controlling the switch which is formed on the fourth conductive layer are separately joined to connection end terminals to the mounting substrate which are electrically separated from each other on the fourth conductive layer.

28. A semiconductor device which mounts a semiconductor chip on a package substrate, wherein

the semiconductor chip includes a digital analogue converter,

the package substrate includes a first conductive layer which is used for connection with pad electrodes of the semiconductor chip, a second conductive layer which is used as the ground plane, a third conductive layer which is used as the power source plane, and a fourth conductive layer which is used for connection with the mounting substrate,

the digital analogue converter includes a circuit which adds a constant current from the constant current source circuit to an output node using a switch,

the semiconductor chip includes a first analog power source terminal and a first analog ground terminal for the constant current source circuit and a second analog power source terminal and a second analog ground terminal for the switch control circuit respectively in a separated manner,

the first analog ground terminal and the second analog ground terminal are connected to analog grounding lines which are separately formed on the first conductive layer, and the respective analog ground lines are connected to the ground plane of the second conductive layer in common, and

the first analog power source terminal and the second analog power source terminal are separately connected to terminals of the fourth conductive layer from the respectively intrinsic analog power source lines which are formed on the first conductive layer via the respective power source planes.

29. An electronic circuit including a first semiconductor device and a second semiconductor device on a mounting substrate, wherein

the mounting substrate includes a plurality of mounting substrate lines which are connected in common with external terminals of a plurality of bits of the first semiconductor device and external terminals of a plurality of bits of the second semiconductor device for every bit,

the mounting substrate lines have lengths thereof from the external terminals of the first semiconductor device to

the external terminals of the second semiconductor device made unequal for respective bits,

assembling lines which reach connecting electrodes of a semiconductor chip from the external terminals of the second semiconductor device have made lengths thereof unequal for respective bits, and

the unequal lengths of the mounting substrate lines have a relationship which offsets the unequal lengths of the assembling lines.

30. A semiconductor device according to claim 29, wherein

the semiconductor chip includes a determination circuit which performs a determination operation using a reference potential supplied from a predetermined pad electrode,

the package substrate includes a first conductive layer which is used for the connection with the pad electrodes of the semiconductor chip, a second conductive layer which is used as a ground plane, a third conductive layer which is used as a power source plane, and a fourth conductive layer which is used for the connection with the mounting substrate, and

the third conductive layer includes a power source plane which is connected with the determination circuit and lines for the reference potential, wherein the lines for the reference potential are arranged in a state that the lines for the reference potential are surrounded by the power source plane.

31. An electronic circuit according to claim 30, wherein the ground plane and the power source plane include specified regions where via holes or through holes are not formed in a penetrating manner with a width equal to or larger than one pitch of external terminals which are arranged on the semiconductor device.

32. An electronic circuit according to claim 31, wherein the first semiconductor device is constituted of a plurality of semiconductor memory devices, and the second semiconductor device is a semiconductor control device which is capable of getting access to and controlling the semiconductor memory devices, wherein

the mounting substrate includes a power source plane of a terminating power source for terminating lines which connect the semiconductor memory devices and the semiconductor control device by way of terminating resistances,

the semiconductor memory devices are mounted closer to the power source plane of the terminating power source than the semiconductor control device,

to the power source plane of the terminating power source, terminating resistances which are connected with the lines and a plurality of first stabilizing capacities which are arranged close to the terminating resistances are connected in a dispersed manner, and

a second stabilizing capacity which is larger than the

first stabilizing capacities is connected to an end portion of the power source plane remote from the supply end which supplies the terminating power source.

33. An electronic circuit according to claim 32, wherein among the lines, the one-way lines having a branch to which a plurality of semiconductor memory devices are connected in common, include lines which have terminating resistances thereof joined to the route having the longer route length starting from the semiconductor control device and lines which have terminating resistances thereof joined to the shorter route in mixture, and

a maximum value of the difference of the route length between the longer route in the one-way line which has the terminating resistance thereof joined to the shorter route and the shorter route is set to a minimum value or less of the difference of the route length between the shorter route in the one-way line which has the terminating resistance thereof joined to the longer route and the longer route.

34. An electronic circuit according to claim 33, wherein

the semiconductor control device includes a semiconductor chip mounted on a package substrate,

the semiconductor chip includes a phase locked loop circuit or a delay locked loop circuit,

the first conductive layer of the package substrate is used for connection with pad electrodes of the semiconductor

chip, and

the first conductive layer includes a power source line which supplies a power source to the phase locked loop circuit or the delay locked loop circuit, and clock lines which supply clock signals to the phase locked loop circuit or the delay locked loop circuit, wherein the power source line and the clock line are spaced apart from each other with a distance larger than a minimum distance size of lines in the first conductive layer.

35. An electronic circuit according to claim 34, wherein

the semiconductor chip includes converters of either one or both of a digital analog converter and an analog digital converter,

on the third conductive layer, power source planes for the converters are separated from the power source plane for other circuits, and

on the first conductive layer, signal lines for converters are formed at positions where the signal lines for converters are overlapped to the power source plane for the converters.

36. An electronic circuit according to claim 35, wherein

the digital analogue converter includes a circuit which adds a constant current from the constant current source circuit to an output node using a switch,

the semiconductor chip includes a first analog power

source terminal and a first analog ground terminal for the constant current source circuit and a second analog power source terminal and a second analog ground terminal for the switch control circuit respectively in a separated manner,

the first analog ground terminal and the second analog ground terminal are connected to analog grounding lines which are separately formed on the first conductive layer, and the respective analog ground lines are connected to the ground plane of the second conductive layer in common, and

the first analog power source terminal and the second analog power source terminal are separately connected to terminals of the fourth conductive layer from the respectively intrinsic analog power source lines which are formed on the first conductive layer via the respective power source planes.